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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/645,389	08/21/2003	Yong Kian Tan	5528US (02-1052.00/US)	8099

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EXAMINER	
BREWSTER, WILLIAM M	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 06/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/645,389	TAN ET AL.	
	Examiner	Art Unit	
	William M. Brewster	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-51* is/are pending in the application.

4a) Of the above claim(s) *16-37 and 46-51* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,5-15 and 38-45* is/are rejected.

7)☒ Claim(s) *2-4* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *082203*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of Group I, Species I, claims 1-15, 38-45 in the reply filed on 11 April 2005 is acknowledged.

Claims 16-36, 46-51 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected group and species, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 11 April 2005.

Information Disclosure Statement

In the IDS received 22 August 2003, only the first page, of the listed two pages has been received and considered.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 7-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Sundstrom et al., US Publication No. 2002/0066523 A1.

Sundstrom anticipates a process for reconstructing a semiconductor wafer, comprising:

fig. 5, forming at least a first alignment droplet and at least a second alignment droplet (see below) from a flowable alignment material at laterally spaced locations on a substrate 25;

placing a first semiconductor die 10 having at least one alignment cavity 24 on a surface 25 thereof such that the at least one alignment cavity of the first semiconductor die makes contact with the at least a first alignment droplet and is positioned by surface tension thereof, p. 2, ¶ 19-22;

placing a second semiconductor die having at least one alignment cavity on a surface thereof such that the at least one alignment cavity of the second semiconductor die makes contact with the at least a second alignment droplet and is positioned by surface tension thereof, in fig. 6, inducing the at least a first alignment droplet and the at least a second alignment droplet to at least partially solidify to maintain positions of the first semiconductor die and the second semiconductor die, wherein although Sundstrom's diagrams only display one bond, the diagrams are heuristic, not drawn are the multiple dies and bonds, p. 2, ¶ 26-28; and

in fig. 7, introducing an underfill material adjacent the surfaces of the first and second semiconductor dice and surrounding the at least a first alignment droplet 16 and the at least a second alignment droplet to form a reconstructed semiconductor wafer;

limitations from claim 5, the process according to claim 1, fig. 6, wherein inducing the at least a first alignment droplet and the at least a second alignment droplet

to at least partially solidify and maintain the positions of the first semiconductor die and the second semiconductor die, p. 2, ¶ 24, comprises at least one of raising or lowering a temperature of the alignment material to at least partially solidify the alignment droplets, p. 2, ¶ 18;

limitations from claim 7, the process according to claim 1, figs. 5-7, wherein placing a first semiconductor die having at least one alignment cavity on a surface thereof such that the at least one alignment cavity of the first semiconductor die makes contact with the at least a first alignment droplet and is positioned by the surface tension thereof comprises placing a semiconductor die having a plurality of alignment cavities on a surface thereto: each of the alignment cavities interacting with a correspondingly positioned alignment droplet to position the semiconductor die, p. 2, ¶ 24-26;

limitations from claim 8, the process according to claim 7, wherein placing a semiconductor die having a plurality of alignment cavities on a surface thereof comprises placing a semiconductor die having a grid pattern of alignment cavities, through the multiple grids, p. 2, ¶ 26-28;

limitations from claim 9, the process according to claim 1, in figs. 6 and 7, wherein introducing an underfill material 16 adjacent the surfaces of the first and second semiconductor dice and surrounding the at least a first alignment droplet and the at least a second alignment droplet comprises introducing the underfill material between the first and second semiconductor dice 10 and the substrate 12 in the form of a fixture plate 16;

limitations from claim 10, the process according to claim 1, further comprising curing the underfill material to a substantially solid state, p. 2, ¶ 25;

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sundstrom as applied to claims 1, 7-10 above, and further in view of Tong et al., US Publication No. 2003/0164555 A1.

Sundstrom does not specify the raising of the temperature for the solidification, but Tong does. Tong teaches:

limitations from claim 5, the process according to claim 1, fig. 6, wherein inducing to at least partially solidify and maintain the positions of the first semiconductor die and the second semiconductor die, comprises at least one of raising or lowering a temperature of the alignment material to at least partially solidify the alignment droplets: to a temperature of 240°C , p. 5, ¶ 30;

limitations from claim 6, the process according to claim 1, wherein inducing the at least a first alignment droplet and the at least a second alignment droplet to at least partially solidify and maintain the positions of the first semiconductor die and the second semiconductor die comprises reacting the alignment material

with an activating agent to at least partially solidify the material: adding imidazole/anyhydride, p. 5, ¶ 30.

Tong gives motivation in p. 1, ¶ 8. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to recognize that combining Tong's process with Sundstrom's invention would have been beneficial because it has minimal residual solvent.

Claims 11-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sundstrom as applied to claims 1, 7-10 above, and further in view of Mountain, US Patent No. 6,013,534.

Sundstrom does not specify backgrinding and singulating the semiconductor dies, but Mountain does. Mountain teaches:

limitations from claim 11, the process according to claim 1, in fig. 16, further comprising singulating the first semiconductor die and the second semiconductor die from the reconstructed semiconductor wafer, col. 7, line 55 - col. 8, line 2;

limitations from claim 12, the process according to claim 11, in fig. 12, wherein singulating the first semiconductor die and the second semiconductor die from the reconstructed semiconductor wafer comprises back-grinding the reconstructed semiconductor wafer to remove the underfill material, col. 7, lines 9-14;

limitations from claim 13, the process according to claim 12, in figs. 11-13, wherein back-grinding the reconstructed semiconductor wafer to remove the

underfill material further comprises removing a fixture plate adhered to the underfill material by back-grinding the reconstructed semiconductor wafer, col. 6, line 65 - col. 7, line 3;

limitations from claim 14, the process according to claim 12, in figs. 5-7, further comprising adhering active surfaces of the first semiconductor die and the second semiconductor die to an adhesive-coated film before singulating, col. 5, line 50 - col. 6, line 5;

limitations from claim 15, the process according to claim 14, in fig. 12, further comprising removing the adhesive-coated film following the back-grinding, col. 7, line 8-14.

Mountain gives motivation in col. 1, line 62 - col. 2, line 14. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to recognize that combining Mountain's process with Sundstrom's invention would have been beneficial because it allows the practitioner to thin only selected dies, as opposed to an entire wafer.

Claims 38-40, 42, 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sundstrom in view of Mountain.

Sundstrom teaches:

a method of performing wafer-level processing on a number of separate semiconductor dice, the method comprising:

selecting a plurality of semiconductor dice, p. 2, ¶ 26-28;

in fig. 5, forming at least one alignment via 24 on a rear surface of each semiconductor die 10 of the plurality;

in figs. 6-7, positioning the semiconductor dice in proper positions to form a semiconductor wafer by placing the at least one alignment via in contact with corresponding alignment droplets positioned on a substrate and using surface tension of the alignment droplets to effect precise alignment of the semiconductor dice, p. 2, ¶ 24-25;

underfilling 16 the positioned semiconductor dice to form a reconstructed semiconductor wafer;

limitations from claim 40, the method of claim 38, in figs. 6-7, wherein positioning the semiconductor dice in proper positions to form a semiconductor wafer by placing the at least one alignment via in contact with corresponding alignment droplets further comprises inducing the alignment droplets to at least partially solidify to maintain the proper positions, p. 2, ¶ 22-24;

limitations from claim 42, the method of claim 38, in figs. 6, 7, wherein the substrate comprises a fixture plate 12 and wherein positioning the semiconductor dice 10 in proper positions to form a semiconductor wafer by placing the at least one alignment via, between 24, in contact with corresponding alignment droplets comprises placing the at least one alignment via in contact with corresponding alignment droplets 14 disposed on the fixture plate, p. 2, ¶ 22-24;

limitations from claim 43, the method of claim 42, in figs. 6, 7, wherein underfilling the positioned semiconductor dice to form a reconstructed semiconductor wafer

comprises introducing an underfill material 16 between the rear surfaces of the semiconductor dice 10 and a surface of the fixture plate 12.

Sundstrom does not specify performing wafer-level processing, but Mountain does. Mountain teaches, in figs. 6-7, selecting the die, and performing wafer-level processing on the reconstructed semiconductor wafer, by thinning, col. 6, line 65 - col. 7, line 14;

limitations from claim 39, the method of claim 38, wherein selecting a plurality of semiconductor dice comprises selecting a number of known functional dice, col. 2, lines 14-34.

Mountain gives motivation in col. 1, line 62 - col. 2, line 14. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to recognize that combining Mountain's process with Sundstrom's invention would have been beneficial because it allows the practitioner to thin only selected dies, as opposed to an entire wafer.

Claim 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sundstrom in view of Mountain as applied to claims 38-40, 42, 43 above, and further in view of Tong.

Neither Sundstrom nor Mountain does not specify the raising of the temperature for the solidification, but Tong does. Tong teaches:

limitations from claim 41, the process according to claim 40, fig. 6, wherein inducing to at least partially solidify and maintain the positions of the first semiconductor die and the second semiconductor die, comprises at least one of raising or lowering a temperature of the alignment material to at least partially solidify the alignment droplets: to a temperature of 240°C , p. 5, ¶ 30;

Tong gives motivation in p. 1, ¶ 8. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to recognize that combining Tong's process with Sundstrom's and Mountain's invention would have been beneficial because it has minimal residual solvent.

Claims 44-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sundstrom in view of Mountain as applied to claims 38-40, 42, 43 above, and further in view of Moden et al., US Patent No. 6,064,221.

Neither Sundstrom nor Mountain specifies wafer-level testing, but Moden does. Moden teaches:

limitations from claim 44, the method of claim 38, in fig. 3, wherein performing wafer-level processing on the reconstructed semiconductor wafer comprises performing a wafer-level testing operation on the reconstructed semiconductor wafer, col. 2, lines 59 - col. 3, line 7;

limitations from claim 45, the method of claim 38, wherein performing wafer-level processing on the reconstructed semiconductor wafer comprises performing

burn-in at the wafer level on the reconstructed semiconductor wafer, col. 4, lines 14 - 52.

Moden gives motivation in col. 2, lines 20-28. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to recognize that combining Moden's process with Sundstrom and Mountain's invention would have been beneficial because it reduces complex mechanical mountain and adhesive spraying arrangements.

Allowable Subject Matter

Claims 2-4 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William M. Brewster whose telephone number is 571-272-1854. The examiner can normally be reached on Full Time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

William M. Brewster

25 May 2005
WB